



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,269	07/08/2003	Anup K. Sharma	SUNMP227	1695
32291	7590	04/27/2006	EXAMINER	
MARTINE PENILLA & GENCARELLA, LLP 710 LAKEWAY DRIVE SUITE 200 SUNNYVALE, CA 94085			CHAUDRY, MUJTABA M	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/616,269	Applicant(s) SHARMA ET AL.	
	Examiner Mujtaba K. Chaudry	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Applicants' response was received February 21, 2006.

- Claims 1-19 are currently pending.
- Rejections under 35 USC 112 in previous office action were never addressed and therefore are maintained.
- Claim objections are withdrawn due to correction in claim 1.

Application pending.

Response to Amendment

Applicant's arguments/amendments with respect to pending claims 1-19 filed February 21, 2006 have been considered but not persuasive. All arguments have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...prior art of record does not teach or suggest a point region configured to indicated an address of the data packet in the memory and transmitting the signal to the pointer region for retransmission of the data packet..." The Examiner respectfully disagrees. A **packet** is defined as a group of data bits which usually consist of header containing control information such as a sequence number, the network address of the station that originated the packet and the network address of the packet's destination. A **pointer** is defined as an identifier that indicates the address or storage location of an data item. Kato clearly teaches, Figure 4 for example, a packet assembly circuit 12 which appends header control information to

Art Unit: 2133

the header by the header addition circuit 20. Therefore the packets transmitted, as taught by Kato, inherently have to have pointer region or header portion of the packet so that the packet is arrived at the appropriate destination and able be requested for retransmission if so needed. See Figure 4, Kato:

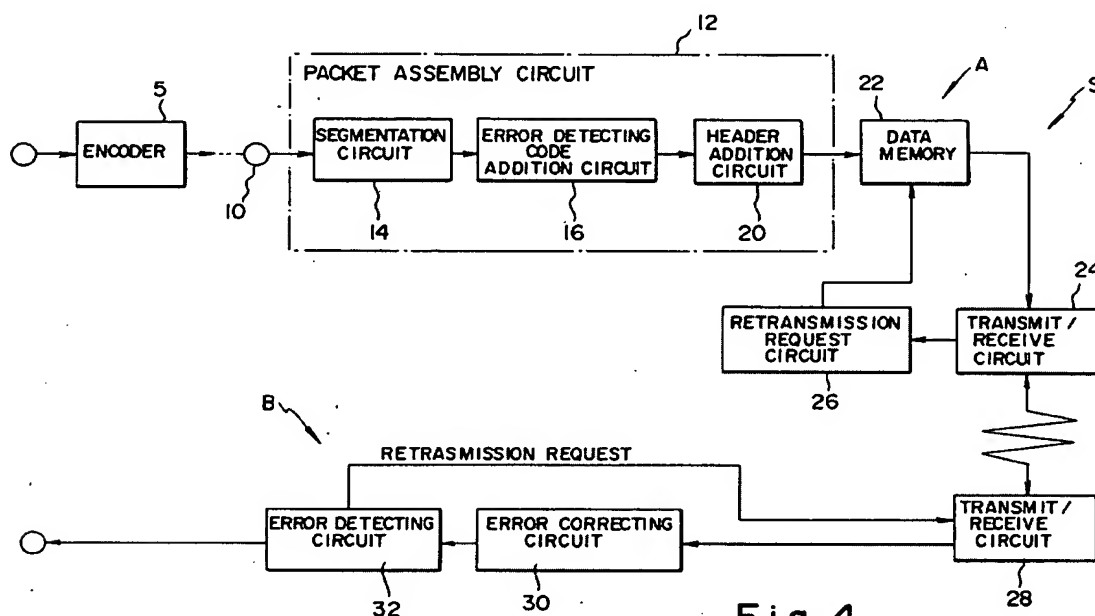


Fig. 4

The Examiner disagrees with the Applicant and maintains rejections with respect to pending claims 1-19. All arguments have been considered. It is the Examiner's conclusion that pending claims 1-19, as presented, are not patentably distinct or non-obvious over the prior art of record. Furthermore, the rejection under title 35 USC 112 is maintained as it was not addressed in Applicants' previous response. See office action:

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In line 7, the phrase, "...appending a first value derived from the data packet to the data packet..." is not clear. It's not clear if the first value is derived from the entire data packet, which includes the header/address portion or just the data portion of the packet. In other words is the first value based solely on the data of the data packet?

Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "...external error checking module..." is not clear since external is a relative term and the claim does not say what it is external to.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Art Unit: 2133

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (USPN 5844918) further in view of (AAPA) Applicant's Admitted Prior Art.

As per claim 1, Kato substantially teaches (abstract) an error correcting code including of basic data and a BCH-based parity code appended thereto is divided into smaller packets. An error detecting code is appended to each of the thus-divided packets, so that transmission basic data is formed. When the transmission basic data is received, the basic data and a BCH-based parity code are derived from the transmission basic data. Error correcting is carried out with respect to the overall transmission basic data. An error detecting operation is carried out with respect to each packet using the error detecting code. If a packet is found to contain errors, a request for retransmission of that packet will be sent to the sending side. In particular, Kato teaches (Figure 4) a communication system with all the essentials of the present application.

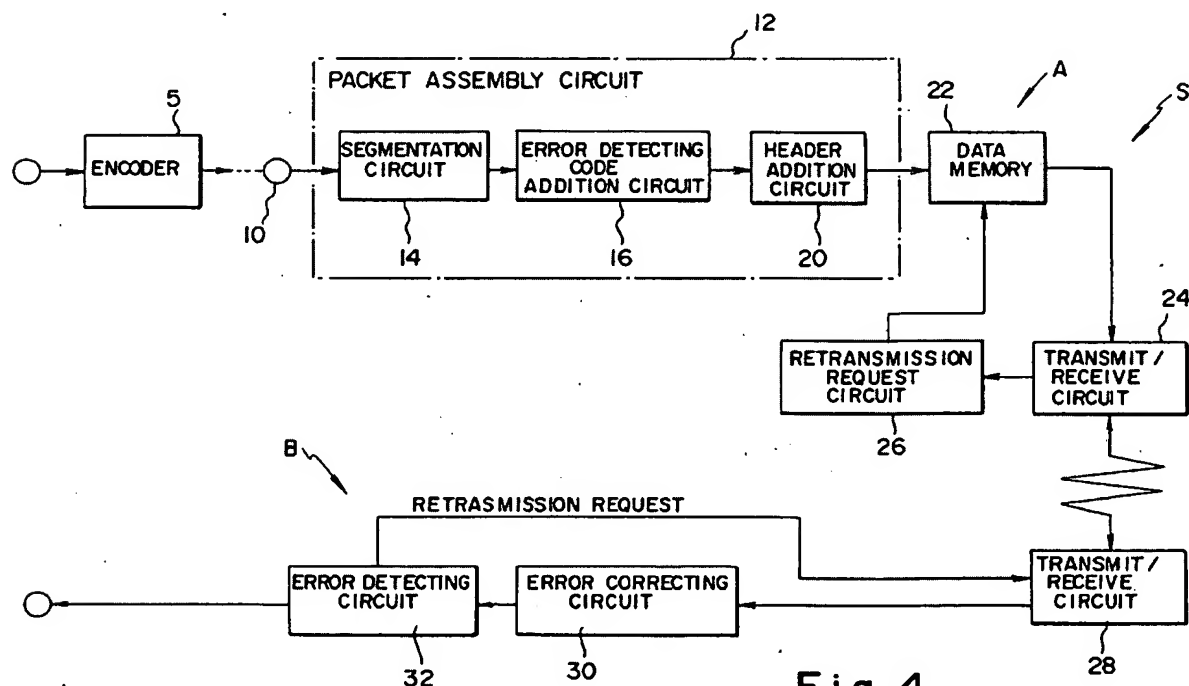


Fig. 4

Kato does not explicitly teach transmitting the data from a first microprocessor to a second microprocessor as stated in the present application.

However, Kato does teach (Figure 4) a communication system which comprises of a transmitter and receiver. The Examiner would like to point out that it is well known in the art that it is inherent for transmitters and receivers to have microprocessors. AAPA also teaches (pages 1-2 and Figure 1) a communication of two microprocessors. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Kato by implementing the communications between two microprocessors. This modification would have been to one of ordinary skill in the art because one of ordinary would have recognized that the communication system in the teachings of Kato and the environment of AAPA are compatible and would have been an efficient way of transmitting digital data from a source A to destination B.

As per claim 2, AAPA substantially teaches, in view of above rejections, the use of appending a CRC (page 1, lines 20-22). The Examiner would like to point out that appending CRC is also taught by Kato (Figure 2c).

As per claim 3, Kato substantially teaches, in view of above rejections, (Figure 9) to detect errors in received data using parity check. The Examiner would like to point out that if the parity check detects an error then it is highly likely that the CRC will be corrupted as stated in the present application.

As per claim 4, Kato substantially teaches, in view of above rejections, (Figure 9, reference number S37) to request for retransmit the packet that is to be retransmitted.

As per claims 5 and 6, Kato substantially teaches, in view of above rejections, (Figure 4) the header addition circuit 120 generates a transmission data packet by further appending a packet header to the data segment complete with the CRC code and the BCH-based parity code, as shown in FIG. 2e. The Examiner would like to point out that the header portion of the packet is well known to include address information.

As per claim 7, Kato substantially teaches (abstract) an error correcting code including of basic data and a BCH-based parity code appended thereto is divided into smaller packets. An error detecting code is appended to each of the thus-divided packets, so that transmission basic data is formed. When the transmission basic data is received, the basic data and a BCH-based parity code are derived from the transmission basic data. Error correcting is carried out with respect to the overall transmission basic data. An error detecting operation is carried out with respect to each packet using the error detecting code. If a packet is found to contain errors, a request for retransmission of that packet will be sent to the sending side. In particular, Kato teaches (Figure.4) a communication system with all the essentials of the present application.

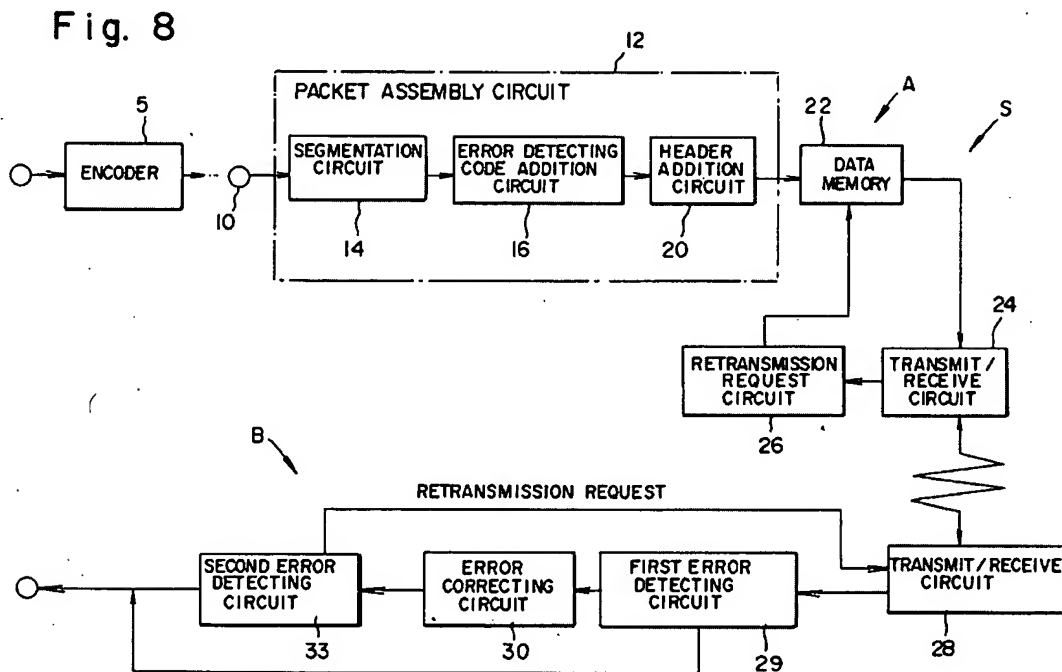
Kato does not explicitly teach transmitting the data from a first microprocessor to a second microprocessor as stated in the present application.

However, Kato does teach (Figure 4) a communication system which comprises of a transmitter and receiver. The Examiner would like to point out that it is well known in the art that it is inherent for transmitters and receivers to have microprocessors. AAPA also teaches (pages 1-2 and Figure 1) a communication of two microprocessors. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Kato by implementing the communications between two microprocessors. This

Art Unit: 2133

modification would have been to one of ordinary skill in the art because one of ordinary would have recognized that the communication system in the teachings of Kato and the environment of AAPA are compatible and would have been an efficient way of transmitting digital data from a source A to destination B.

As per claim 8, Kato substantially teaches, in view of above rejections, (Figure 8) to detect errors in first error detecting circuit 29.



As per claim 10, Kato substantially teaches, in view of above rejections, (Figure 8, reference number S14) to request for retransmit the packet that is to be retransmitted. The Examiner would like to point out that the segmentation circuit 14 serializes the data prior to transmission.

As per claims 9 and 11, Kato substantially teaches, in view of above rejections, (Figure 4) the header addition circuit 120 generates a transmission data packet by further appending a

Art Unit: 2133

packet header to the data segment complete with the CRC code and the BCH-based parity code, as shown in FIG. 2e. The Examiner would like to point out that the header portion of the packet is well known to include address information.

As per claim 12, Kato substantially teaches, in view of above rejections, (Figure 9, reference number S37) to request for retransmit the packet that is to be retransmitted.

As per claim 13, AAPA substantially teaches, in view of above rejections, the use of appending a CRC (page 1, lines 20-22). The Examiner would like to point out that appending CRC is also taught by Kato (Figure 2c).

As per claim 14, Kato substantially teaches (abstract) an error correcting code including of basic data and a BCH-based parity code appended thereto is divided into smaller packets. An error detecting code is appended to each of the thus-divided packets, so that transmission basic data is formed. When the transmission basic data is received, the basic data and a BCH-based parity code are derived from the transmission basic data. Error correcting is carried out with respect to the overall transmission basic data. An error detecting operation is carried out with respect to each packet using the error detecting code. If a packet is found to contain errors, a request for retransmission of that packet will be sent to the sending side. In particular, Kato teaches (Figure 4) a communication system with all the essentials of the present application.

Kato does not explicitly teach transmitting the data from a first microprocessor to a second microprocessor as stated in the present application.

However, Kato does teach (Figure 4) a communication system which comprises of a transmitter and receiver. The Examiner would like to point out that it is well known in the art that it is inherent for transmitters and receivers to have microprocessors. AAPA also teaches

Art Unit: 2133

(pages 1-2 and Figure 1) a communication of two microprocessors. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Kato by implementing the communications between two microprocessors. This modification would have been to one of ordinary skill in the art because one of ordinary would have recognized that the communication system in the teachings of Kato and the environment of AAPA are compatible and would have been an efficient way of transmitting digital data from a source A to destination B.

As per claim 15, Kato substantially teaches, in view of above rejections, (Figure 4) the header addition circuit 120 generates a transmission data packet by further appending a packet header to the data segment complete with the CRC code and the BCH-based parity code, as shown in FIG. 2e. The Examiner would like to point out that the header portion of the packet is well known to include address information.

As per claim 16, Kato substantially teaches, in view of above rejections, (Figure 9, reference number S37) to request for retransmit the packet that is to be retransmitted.

As per claim 17, Kato substantially teaches, in view of above rejections, (Figure 8, reference number S14) to request for retransmit the packet that is to be retransmitted. The Examiner would like to point out that the segmentation circuit 14 serializes the data prior to transmission.

As per claims 18-19, AAPA substantially teaches, in view of above rejections, the use of appending a CRC (page 1, lines 20-22). The Examiner would like to point out that appending CRC is also taught by Kato (Figure 2c).

Art Unit: 2133

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.



Mujtaba Chaudry
Art Unit 2133
April 20, 2006



ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100